REMARKS

Claims 1-4, 6-15, 17-21 and 23-32 were pending in the application with all claims rejected.

Claims 1-2, 4, 7-8, 23-14, 18, 20, 24-25, and 31 are amended to place the claims in better form for appeal. Claims 3 and 23 have been cancelled.

Reconsideration and allowance of all claims, or to resolve additional issues upon appeal, is respectfully requested.

No New Matter – Claim Temperature Limitations Have Reverted to Original

The Examiner has objected to the amendment filed August 16, 2002 under 35 USC 132 on the grounds that claims incorporating the step of a pre-annealing at a range of between 350 ~ 499°C is unsupported in the originally filed specification. The pre-annealing temperature limitations of 350 ~ 750°C have been reinstated in the claims. Applicant respectfully requests, therefore, that the new matter rejection and those related to 35 U.S.C. §112, first paragraph, should now be respectfully withdrawn.

Claims Rejections – 35 USC § 112, second paragraph

Claims 1-4, 6-16, 17-21, and 23-32 have been rejected under 35 U.S.C. 112, second paragraph, in view of amendments to claims 8 and 31. In particular, the Examiner refers to the specification which states (page 7, lines 15-16) that "the crystallization annealing is preformed preferably at about **650° C**" and (page 7, lines 5-7) "the pre-annealing step is preferably preformed at a **higher temperature** than the temperature of the crystallization annealing step." The Examiner continues that these statements indicate that the invention is different from what is defined in the claim(s) because the new matter added include: "the pre-annealing is preformed at a range of between 350 ~ 499° C", which limitation has now reverted to the original temperature range of 350 ~ 750°C.

The statements are not at odds because the specification discloses several different pre-annealing criteria (page 6, lines 32-33) in a range of 350-750° C. The annealing and crystallization in the example referred to on page 7, lines 10-23 (see, also, page 7, lines 2-3) is performed in a nitrogen atmosphere where thermal pre-annealing is preformed preferably at about 700° C. Under a mixed atmosphere (page 7, lines 3-5) the thermal pre-annealing is

performed preferably at only about 450° C. As the application contains claims to different embodiments of the invention, the claims are not contradictory with the specification disclosure and applicants respectfully request that the §112 rejections be removed.

Claims Rejections – 35 USC § 102(e) and §103(a)

Claims 1-3, 6, 8-15, 17, 19-23 and 27 are rejected under 35 U.S.C 102(e) as being clearly anticipated by Agarwal et al. (U.S. Pub No. 2002/0037630) (cited previously). Applicant noted in its response to the first Office Action the following:

> The Examiner states in paragraphs 1 and 2 of the Office Action the following, "Agarwal further teaches that the capacitor dielectric layer (28) is annealed, thus crystallized." Applicant respectfully disagrees with this statement. Instead, after careful review of the Agarwal '630 reference, Applicant can find no such specific recitation or suggestion within the reference regarding the use of a crystallized dielectric. Instead, paragraph 0048 of Agarwal '630 states only that the dielectric should have a high dielectric constant around 9, and that it be conformally formed as a "thin layer" over the enhanced surface area electrode (26) so that it preferably provides an enhanced surface area on a surface facing away from the bottom electrode. Paragraph 0055 states, in fact, that the anneal process is typically performed before the dielectric layer and second electrode are formed. And paragraph 0056 simply lists the suitable dielectric materials available.

The substance of the rejection in the Final Office Action is nearly identical to that of the earlier Office Action with the exception that the Examiner has noted (presumably in response to applicant's above arguments) that, "[r]egarding the crystallized material, annealing the dielectric layer (28) is inherently crystallized the dielectric layer." The Examiner recites the Narwanka '203 patent as supporting this proposition.

The Examiner's characterization of Narwanka '203 as supporting the proposition that "annealing the capacitor dielectric layer following its deposition inherently crystallizes it" is incorrect. Instead, Narwanka '203 states clearly that the substrate is exposed to an intermediate anneal step that occurs at a temperature less than the crystallization temperature of the dielectric. (col. 6, lines 62-64) Furthermore, the "crystallization temperature" is defined within Narwanka '203 (col. 7, lines 5-7) as "a temperature at which an amorphous or substantially amorphous metal oxide dielectric is converted to a polycrystalline film." Annealing therefore does not always crystallize the dielectric unless the annealing temperature is at or above the crystallization temperature.

Crystallization of such materials typically occurs at relatively high temperatures. The Narwanka '203 patent states (col. 8, lines 27-29) that "an amorphous tantalum pentaoxide film can be given a crystallization anneal by heating substrate 200 to a temperature between 750°-850°C. Agarwal mentions crystallization only once (paragraph 0039), and that is in reference to the treatment of a surface-enhanced electrode. It can be realistically presumed, therefore, that Agarwal would mention crystallization of the dielectric if in fact that was the intent of the teachings. However, nowhere in Agarwal does it mention crystallization of the dielectric layer. It cannot be assumed, therefore, that one knowledgeable in the art would read Agarwal to teach the pre-annealing of a lower electrode and a crystallization of the dielectric.

Claims 6, 8, 17 and 23 include the further limitation that the pre-anneal process does not change the materiality of the lower electrode. The process taught in Agarwal, however, clearly changes the materiality of the lower electrode. Paragraph 0035 discloses that the ruthenium oxide layer 12 is at least partially converted to ruthenium. Accordingly, the present invention as stated in claims 6, 8, 17 and 23 is clearly different from that taught in Agarwal. Accordingly, applicant respectfully requests that the Examiner's rejection of claims 6, 8, 17 and 23 be removed.

The remaining claims have been rejected under 35 USC §103(a) as being unpatentable over Agarwal '630 alone and in view of Aoki '952. Although Aoki includes the term "crystallization annealing" (col. 4, lines 63), the technologies employed in Aoki and Agarwal are quite different and the end product unrelated except that both are directed to the very broad field of semiconductor manufacturing. In fact, Aoki does not mention "leakage current" nor "capacitance" once and thus one with knowledge of the Agarwal '630 reference would not think to combine the teachings therein with those of Aoki '952 to solve the leakage current problems and capacitance issues addressed by the present invention (see experimental advantages of invention in FIGs. 3A-7B). The courts have continuously cautioned the PTO from making the same types of hindsight combinations that are made here: see In re Rouffett, 47 USPQ2d 1453 (Fed. Cir. 1998); Ecolochem v. Southern Cal. Edison, 56 USPQ2d 1065 (Fed. Cir. 2000); and In re Kotzab, 55 USPQ2d 1313 (Fed. Cir. 2000). Furthermore, the courts have recently reiterated the rule that a combination of two prior art references without the specific hint or suggestion in the particular references to support the combination, even where "common knowledge" or "common sense" is imputed, is improper. In re Lee, 61 USPQ2d 1430 (Fed. Cir. 2002).

Further Distinctions Between Claimed Invention and Prior Art

Claims 1-2, 7-8, 23-14, 18, 20, 24-25, and 31 have also been amended to highlight those elements that are novel and nonobvious over the prior art.

The independent claims, particularly claims 1, 13, and 20, have been amended to recite that the lower electrode is a metal and eliminates reference to a metal oxide. A metal oxide would have an enhanced surface area whereas a metal would not. This differs from the Agarwal reference in which the lower electrode is taught to include an enhanced surface area. The material of the lower electrode of the invention thus differs from that of the Agarwal reference. Claims 2 and 14 further limit the lower electrode material to either ruthenium (Ru) or platinum (Pt) which is supported in page 6, lines 15-26 of the specification.

The independent claims are further amended to recite the use of and subsequent removal of carbon from the lower electrode. The purpose of the pre-annealing is to remove the impurities (carbon) for preventing crystallization formed in the lower electrode. This contrasts with the annealing step in the Agarwal reference whose purpose is to change the form of the surface of the lower electrode. The language of the claims as amended include an expression stating that the purpose for pre-annealing is to remove the impurities (carbon) for preventing crystallization within the lower electrode. Support for the limitation can be found on page 11, lines 27-29 of the specification.

A further limitation, that of performing a "crystallization annealing" can be found in amended claims 7, 18, and to a more specific extent independent claim 20. Referring to the crystallization annealing of the capacitor dielectric layer, by the pre annealing, the crystallization temperature of the capacitor dielectric layer is lowered (see, e.g., page 7, line 16). That is, since the capacitor dielectric layer is grown along a grain boundary of the pre-annealed lower electrode, the capacitor dielectric layer becomes partially crystallized. This partial crystallization decreases the crystallization temperature. When the temperature of the crystallization of the capacitor dielectric layer is lowered, the leakage current substantially decreases, which is well known in the art. Such a matter is one of the features of the present invention. Therefore, the claims have been amended to reflect that the crystallization of the capacitor dielectric layer starts at a ***lower*** temperature than the *inherent crystallization* temperature of the capacitor dielectric layer (also claim 24).

In claims 20 in particular, the capacitor dielectric layer claimed is a tantalum oxide layer. The inherent crystallization temperature of a tantalum oxide layer is over 700 C; however, the crystallization temperature of the tantalum oxide layer in the present invention is about 650 C. In contrast, the capacitor dielectric layer in the Aoki reference is PZT and the inherent crystallization temperature of PZT is about 650 C. Also, the Agarwal and Aoki references fail to disclose the crystallization of the capacitor dielectric layer at a lower temperature than the inherent crystallization temperature of the capacitor dielectric layer. Therefore, the crystallization temperature of the present invention differs from that of the Aoki reference.

In summary, this invention differs from the cited references in the aspects of the material of the lower electrode, the purpose of the pre annealing, and the crystallization temperature used compared to the inherent crystallization temperature of the material treated.

CONCLUSION

For the foregoing reasons, reconsideration and allowance of all pending claims of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please cancel claims 3 and 23 and amend the remaining claims as follows:

1. (Twice amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate using a source having carbon;

subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode, wherein the pre-annealing is a thermal annealing under a selected atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode [, wherein the capacitor dielectric layer is formed of a crystalline material]; and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal.

2. (Twice amended) The method of claim 1, wherein the lower electrode is formed of a material selected from the group consisting of ruthenium and platinum [a metal and a metal oxide].

4. (Once amended) The method of claim 1 [3], wherein a metal organic material is used as a source of the CVD method.

7. (Twice amended) The method of claim 1 [4], wherein the step of forming a capacitor dielectric layer comprises:

depositing [forming] a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a [processing] temperature of the crystallization annealing is lower than an inherent temperature of crystallization annealing of said capacitor dielectric layer [pre-annealing is higher than that of the crystallization annealing].

8. (Twice amended) The method of claim 6, wherein the pre-annealing is performed at a range of between 350 ~ [499] 750°C.

13. (Twice amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate by CVD method using a source having carbon;

subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode, wherein the pre-annealing is a treatment exposing the lower electrode under a plasma atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode [, wherein the capacitor dielectric layer is formed of a crystalline material]; and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal.

14. (Twice amended) The method of claim 13, wherein the lower electrode is formed of a material selected from the group consisting of ruthenium and platinum [a metal and a metal oxide, and the lower electrode is formed by a CVD method].

18. (Twice amended) The method of claim 13 [15], wherein the step of forming a capacitor dielectric layer comprises:

depositing [forming] a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a [processing] temperature of the crystallization annealing is lower than an inherent temperature of crystallization annealing of said capacitor dielectric layer [pre-annealing is higher than that of the crystallization annealing].

20. (Twice amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate [, wherein the lower electrode is formed] by a CVD method using a source having carbon [, and wherein the lower electrode is formed of a material selected from the group consisting of a metal and a metal oxide];

subjecting the lower electrode to a pre-annealing form removing carbon remaining in the lower electrode, wherein the pre-annealing is a treatment exposing the lower electrode under plasma atmosphere;

depositing a tantalum oxide layer on the pre-annealed lower electrode;

crystallizing the tantalum oxide layer;

[forming a capacitor dielectric layer on the pre-annealed lower electrode, wherein the capacitor dielectric layer is formed of a crystalline material;] and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal, the pre-annealing is performed at a range of between 350 ~ 750°C, and the materiality and surface form of the lower electrode does not substantially change be the pre-annealing.

24. (Twice amended) The method of claim 21, wherein a temperature of the crystallization annealing is lower than the inherent temperature of crystallization of said capacitor dielectric layer [the step of forming a capacitor dielectric layer comprises:

forming a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a processing temperature of the pre-annealing is higher than that of the crystallization annealing].

25. (Once Amended) The method of claim 24, wherein the inherent crystallizing temperature of the tantalum oxide layer is over 700°C and the crystallizing temperature of the tantalum oxide layer [processing temperature of crystallization annealing] is about 650°C.

31. (Once Amended) The method of claim 17, wherein the pre-annealing is performed at a range of between 350 ~ [499] 750°C.